U.S. Express Mail Label EL 752587395 US

09/857503
JC18 Rec'd PCT/PTO 0 1 JUN 2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

8/11 #9 4/8/02

In Re Application:	Andrew Dewhurst	Examiner:	Unassigned
Serial No.	Unassigned	Group Art Unit:	Unassigned
Filing Date:	Herewith	Attorney Docket No.	078986/0203
Title:	A SERIAL-PARALLEL BINARY MULTIPLIER		

CERTIFICATE UNDER 37 CFR 1.8: I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on June 1, 2001.

Richard S. Ruggiero

Richard S. Ruggiero

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, DC 20231

Dear Sir:

Prior to the first Office Action, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please amend the specification, at page 2, after line 9, to add the following paragraphs:

US-A-5539685 describes the conventional process of multiplication by repeated shift and add operations. An improved high-speed multiplier device is then described. The improved devices requires both the operands to be loaded into separate register before the shift and addition process is commenced. The latter process is first completed before the partial process product is stored in a temporary register. Since each process is dependent on the previous process being complete, the multiplication operation is still relatively time consuming.

In Computer Design (Pennwell Publ. - US ISSN 00104566) Volume No. 5, May 1972,Pages 115-121, XP-002130443 an article entitled "2's Complement Arithmetic Operations" by S. Sklar describes the technique of Booth Coding for 2's complement multiplication. This technique provides a multiplication process with performance improvements. An arithmetic operation is performed on one operand by reference to decoded bits of a second operand. The required arithmetic operation is determined by the results of the decoding process.